Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.106”**

**.077”**

**GATE**

**.017 X .025”**

**SOURCE**

**.018 X .024”**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: .017” X .024” min.**

**Backside Potential: DRAIN**

**Mask Ref: GEN 3**

**APPROVED BY: DK DIE SIZE .077” X .106” DATE: 9/6/18**

**MFG: INT’L RECTIFIER THICKNESS .019” P/N: IRFC310B**

**DG 10.1.2**

#### Rev B, 7/1